Remarks

Claims 1, 3, 4, 7, 10-18, and 20 are pending in this application. Claims 2, 5, 6, 8, 9, and 19 were previously cancelled. Claims 1, 7, and 17 were previously amended. The Examiner has rejected claims 1, 4, and 6 under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent Publication No. 2003/0046464 to Murty et al. (hereinafter "Murty") in view of U.S. Patent No. 4,370,720 to Hyatt (hereinafter "Hyatt"). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty in view of U.S. Patent No. 5,809,314 to Carmean et al. (hereinafter "Carmean"). Further, claims 7, 8, 10-15, 17, 19, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of Hyatt and further in view of U.S. Patent No. 6,857,084 to Giles (hereinafter "Giles"). Finally, claims 16 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty/Hyatt in view of Giles, and further in view of Carmean.

A. Remarks Regarding Rejection of Claims 1, 3, and 4 Under 35 U.S.C. § 103

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The combination of Murty and Hyatt fails to teach or suggest all the claim limitations of independent claim 1. Specifically, the combination fails to teach or suggest that "the interrupt handling processor assigned to perform the processing tasks associated with the interrupt **initiates** the release of the non-interrupt handling processors from the interrupt mode."

Rather, Murty teaches that one of the logical processors is the first to access the shared register and handles the interrupt. Murty at [0049]. The rest of the "logical processors detect that the interrupt has been claimed and return from the interrupt-handler." Murty at [0049]. Murty does not disclose that the first processor "initiates" the release of the other processors. Murty teaches that the other processors detect that another processor is handling the interrupt and "return" from the interrupt handler. Murty at [0049].

Murty also fails to disclose a "timed release basis" for releasing the non-interrupt handling processors so as to release them from the interrupt mode serially. Murty discloses resetting a flag and merely states that the "time between common interrupts is typically greater than the time necessary for all of the logical processors to execute the interrupt handler ... and access the flag." Murty at [0046]. Murty does not mention a time delay between releasing processors. The time referenced in Murty relates to the time between typical interrupts and *not* the time delay associated with releasing the non-interrupt handling processors so as to reduce contention for system resources as required by independent claim 1.

Further, Murty does not disclose the successive serial release of logical processors from the interrupt mode "so as to reduce contention by the non-interrupt handling processors for system resources" as required by claim 1. Examiner states that the "order of operation for tasks handled by all the processors will also occur in the same 1 to n order" where 1 to n is the label given to the processors to indicate that more than one processor is contemplated. Office Action at 4. However, Murty does not discuss the processors registering a common interrupt for logical processors 120(1) - 120(n) in any particular order nor does it discuss releasing them in any particular order. Murty denotes that element 120 is a processor and identifies that any number of processors can exist by labeling the processors with the common notation of (1) to (n). Murty at

Figure 1. In fact, Murty discloses that any processor could be the first processor to access ICR 150 and complete the processing of the interrupt. Murty at [0027]. Murty merely states that after the first processor has accessed the ICR 150 the remaining processors "resume execution of their threads." Murty at [0027]. Murty states that "[t]he remaining logical processors read the second value, which directs them to exit the interrupt-handler." Murty at [0049]. Murty does not discuss that these processors are released serially or that they will be released in consecutive order. In fact, the processors cannot be released in a pure consecutive order as any of the 1 to n processors could be the processor that is handling the interrupt. Murty even discloses that "each processor, acting independently, [determines] whether or not it is responsible for handling the common interrupt." Murty at [0034]. Murty describes this handling of interrupts as a "race-to-flag mechanism" and does not require that the processors act consecutively or serially. Murty at [0034].

Also, Hyatt does not disclose non-interrupt handling processors being serially released as required by claim 1. Hyatt is directed to "a numerical control system for machine control using a stored program data processor; particular for coordinate resolution of motion commands." Hyatt at 3:6-9. Hyatt describes the operation of a data processor for performing micro-operations. Hyatt at 19:46-55. The processor responds to a series of flip-flops that indicate the next micro-operation. Hyatt at 19:66-20:25. For instance, an X5 signal indicates that an external interrupt has occurred, whereupon the data processor ignores it unless certain flip-flops are in certain states. Hyatt at 18-25. The cited portion of Hyatt by Examiner does not discuss a non-interrupt handling processor at all. The description in Hyatt of a data processor responding to flip-flops is not the same as the requirements of claim 1.

Because all of the elements of independent claim 1 are not taught or suggested by the combination of Murty and Hyatt, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Hyatt, all of the claimed limitations of independent claim 1 are not shown in the combination. Applicant respectfully submits that the rejection of claim 1 should be withdrawn and that this claim should be passed to issuance. Claims 3 and 4 each depend directly or indirectly from independent claim 1 and are therefore requested to be passed to issuance for at least the same reasons.

B. Remarks Regarding Rejection of Claims 7, 8, 10-15, 17, 19, and 20 Under 35 U.S.C. § 103

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The combination of Murty and Hyatt in view of Giles fails to teach or suggest all the claim limitations of independent claims 7 and 17. Specifically, Murty in view of Hyatt in further view of Giles fails to teach "**initiating the serial exit** of the non-interrupt handling processors from interrupt mode" as required by claims" as required by claim 17 and similarly by claim 7 for at least the same reasons stated above with respect to claim 1.

With respect to claims 11, 12, and 17, Giles fails to disclose "determining whether each non-interrupt handling processor was in a halt state immediately before entering the mode." Giles discusses that processors are placed in a debug mode "without an excessive time delay to preserve the states of the processors for multiprocessor debug by **halting all of the processors at approximately the same time**." Giles at 2:32-35. Giles teaches placing every processor in the halt state regardless of the prior state. This is not the same as determining if a "non-interrupt handling processor was in a halt state immediately before entering the mode" as required by these claims.

Because all of the elements of independent claims 7 and 17 are not taught or suggested by the combination of Murty in view of Hyatt in further view of Giles, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Hyatt, all of the claimed limitations of independent claims 7 and 17 are not shown in the combination. Applicant respectfully submits that the rejection of claims 7 and 17 should be withdrawn and that these claims should be passed to issuance. Claims 10-16, 18, and 20 each depend directly or indirectly from independent claims 7 and 17 and are therefore requested to be passed to issuance for at least the same reasons.

C. No Waiver

All of Applicant's arguments and amendments are without prejudice or disclaimer. Additionally, Applicant has merely discussed example distinctions from the cited references. Other distinctions may exist, and Applicant reserves the right to discuss these additional distinctions in a later Response or on Appeal, if appropriate. By not responding to

additional statements made by examiner, Applicant does not acquiesce to examiner's additional statements, such as, for example, any statements relating to what would be obvious to a person of ordinary skill in the art. The example distinctions discussed by Applicant are sufficient to overcome the anticipation rejections.

Conclusion

Applicant respectfully submits that the pending claims 1, 3, 4, 7, 10-18, and 20 of the present invention are allowable. Applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

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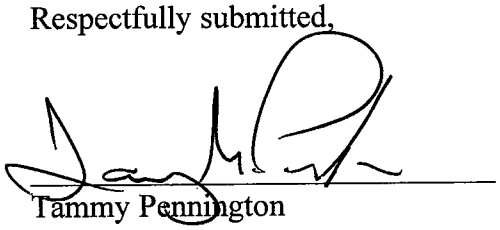
Respectfully submitted,



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